SSC8012GN2

N-Channel Enhancement Mode MOSFET

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
16V	±12V	12mΩ@10V	12A
		15mΩ@4V5	

➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

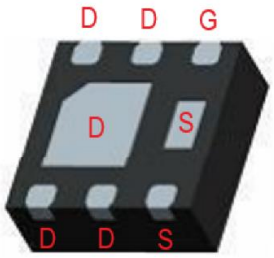
➢ Applications

- Load Switch
- Portable Devices
- DCDC Conversion
- Charging

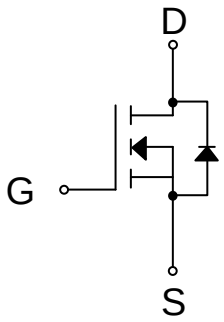
➢ Ordering Information

Device	Package	Shipping
SSC8012GN2	DFN2020-6L	3000/Reel

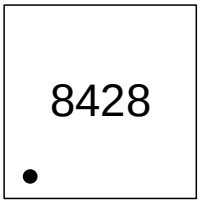
➢ Pin Configuration



DFN2020-6L (Bottom View)



Pin Configuration



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Ratings	Unit
Drain-to-Source Voltage		V_{DS}	16	V
Gate-to-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [d]	T_C=25℃	I_D	12	A
	T_C=100℃		7	
Pulsed Drain Current [b]		I_{DM}	40	A
Power Dissipation [c]	T_C=25℃	P_D	3.1	W
	T_C=100℃		1.25	
Operation junction temperature		T_J	-55~150	℃
Storage temperature range		T_{STG}	-55~150	

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	$R_{\theta JA}$	40	℃/W

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

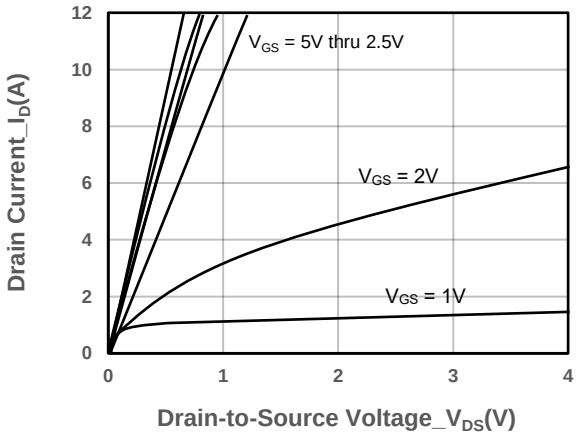
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

d. The maximum current rating is package limited.

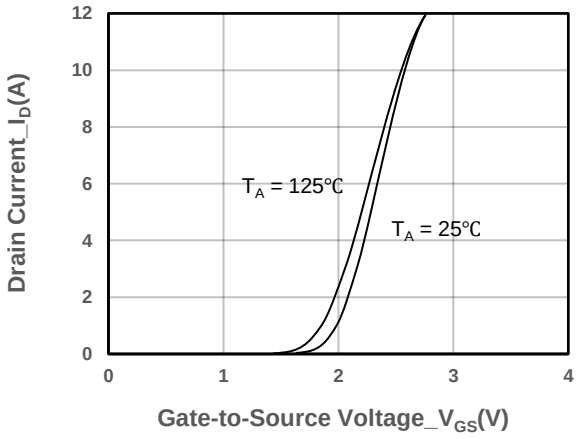
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	16			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.4	0.75	1.2	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 6A		12	16	mΩ
		V_{GS} = 2.5V, I_D = 3A		15	20	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 1A			1.3	V
Input Capacitance	C_{ISS}	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz		870		pF
Output Capacitance	C_{OSS}			300		
Reverse Transfer Capacitance	C_{RSS}			140		
Total Gate Charge	Q_G	V_{GS} = 4.5V, V_{DS} = 10V, I_D = 5A		8.6		nC
Gate to Source Charge	Q_{GS}			1.9		
Gate to Drain Charge	Q_{GD}			2.2		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = 4.5V, V_{DS} = 10V, R_L = 1.4Ω, R_G = 6Ω, I_D = 5A		6		ns
Rise Time	T_r			12		
Turn-off Delay Time	$T_{D(OFF)}$			46		
Fall Time	T_f			22		

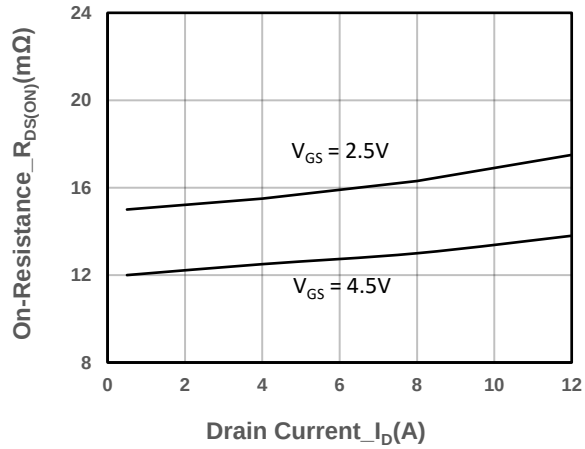
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



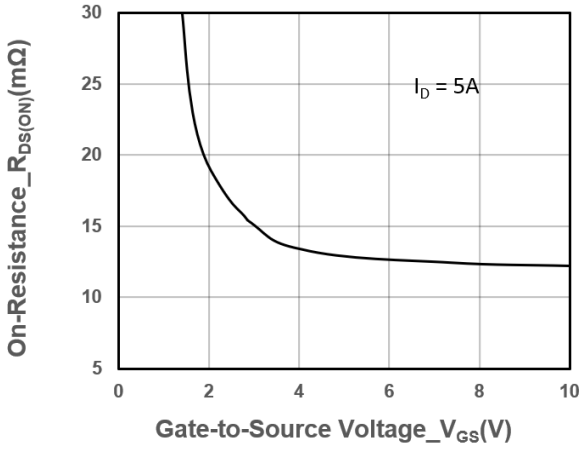
Output Characteristics



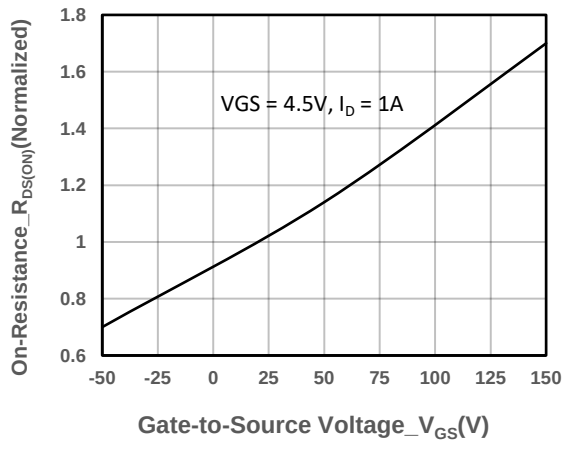
Transfer Characteristics



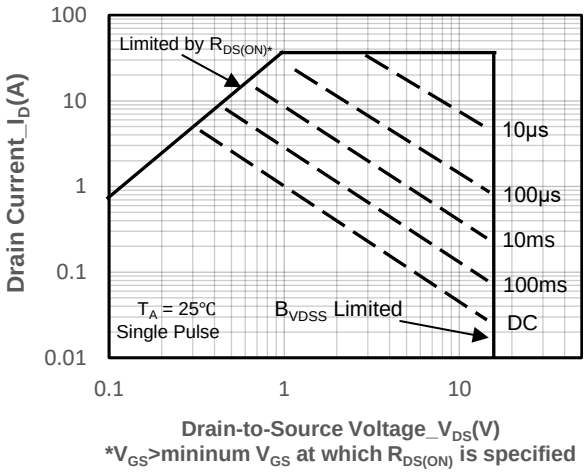
On-Resistance vs. Drain Current and Gate Voltag



On-Resistance vs. Gate-to-Source Voltage

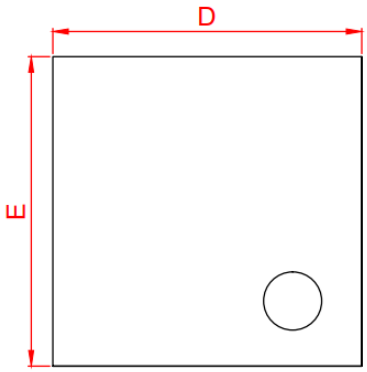


On-Resistance vs. Junction Temperature

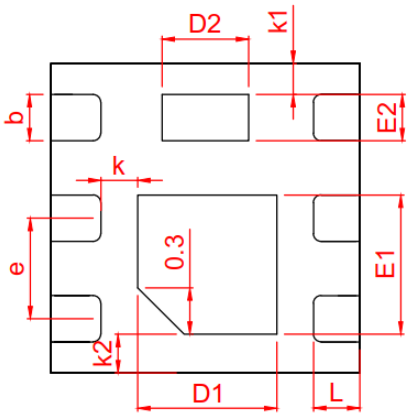


Safe Operating Area vs. Junction-to-Ambient

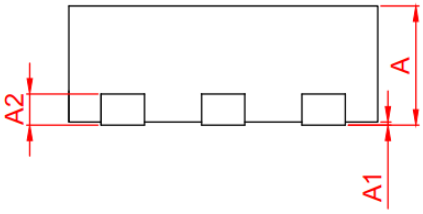
➢ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
* A1	0.00	0.02	0.05
* b	0.25	0.30	0.35
* A2	0.152 BSC		
* D	1.95	2.00	2.05
* E	1.95	2.00	2.05
* E1	0.80	0.90	1.00
* E2	0.25	0.30	0.35
* D1	0.80	0.90	1.00
* D2	0.46	0.56	0.66
* e	0.65 REF		
* L	0.25	0.30	0.35
* K	0.20	0.25	0.30
* K1	0.15	0.20	0.25
* K2	0.20	0.25	0.30

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